CLAIMS

1. A PCI Express to PCI bridge comprising:

a PCI interface couplable to a PCI bus having PCI compatible devices connected thereto;

a port arbitration circuit for controlling the PCI compatible devices to guarantee bandwidth to upstream data sent from a predetermined one of the PCI compatible devices and for allocating the data to a predetermined one of a plurality of virtual cannels supported by PCI Express,

a virtual channel arbitration circuit for allocating the virtual channels to an output port of the bridge; and

a PCI Express interface coupled between the virtual channel arbitration circuit and the output port.

2. The bridge of Claim 1 further comprising a port arbitration table coupled to the port arbitration circuit, the port arbitration table determining PCI bus transactions to guarantee isochronism of data transfers.

3. The bridge of Claim 2 further comprising a bus traffic management circuit responsive to the control data stored in the port arbitration table for controlling the port arbitration circuit.

4. The bridge of Claim 1 further comprising a PCI bus arbiter circuit couplable to a PCI bus for controlling access by PCI compatible devices to the PCI bus.

5. The bridge of Claim 3 further comprising a PCI bus arbiter circuit couplable to a PCI bus for controlling access by PCI compatible devices to the PCI bus.

6. The bridge of Claim 5 wherein the PCI bus arbiter grants control of the PCI bus to a PCI compatible device connected to the bus, the PCI bus arbiter being controlled by the bus traffic management circuit to grant control of the PCI bus to a PCI compatible device sending isochronous data at predetermined intervals to maintain the isochronism of the data.

7. The bridge of Claim 1 further comprising an upstream virtual channel window control register, the register being addressed by a PCI compatible device for sending isochronous data.

8. The bridge of Claim 7 wherein the window control register is located within PCI Express configuration space.

9. The bridge of Claim 7 wherein the window control register is located within extended PCI configuration space.

10. The bridge of Claim 7 wherein the window control register is located in memory.

11. The bridge of Claim 10 wherein the memory is located within the bridge.

12. The bridge of Claim 11 wherein the memory is located in memory mapped configuration space.

13. The bridge of Claim 1 further comprising a virtual channel arbitration circuit.

14. The bridge of Claim 1 wherein the upstream data is isochronous data.

15. The bridge of Claim 14 wherein the PCI compatible device is an IEEE 1394 device.

16. A method for isochronous transfer of data from a PCI compatible device connected to a PCI bus to a PCI Express fabric comprising:

receiving data at an input port for isochronous transfer from a preselected PCI compatible device;

controlling PCI compatible devices on the PCI bus to guarantee bandwidth from the preselected PCI device;

allocating the data from the preselected device to one of a plurality of virtual channels supported by PCI Express;

arbitrating the virtual channels onto an output port.

17. The method of Claim 16 wherein controlling PCI compatible devices on the PCI bus is in response to control signals generated in response to a port arbitration table.

18. The method of Claim 16 further comprising:

writing data from a PCI compatible device to a register defined in a PCI Express to PCI bridge to define the data transfer as isochronous.

19. A method for isochronous transfer of data between a PCI compatible device and PCI Express fabric comprising:

receiving data from a PCI compatible device connected to a PCI bus, the data being addressed to a register defined in a PCI Express to PCI bridge;

transferring the data addressed to the register upstream to a PCI Express fabric, the data transfer maintaining isochronism of the data.

20. A PCI Express to PCI bridge comprising:

first means for receiving data from a PCI compatible device connected to a PCI bus and sending the data upstream to a CPU via a PCI Express fabric, the first means maintaining isochronism of isochronous data from the PCI compatible device, and

second means for receiving isochronous data from the CPU via the PCI Express fabric and for sending the data downstream to the PCI compatible device, the second means maintaining isochronism of the data.